AMENDMENTS TO THE CLAIMS

1. (ORIGINAL) An apparatus comprising:

a plurality of writeable registers configured to store (i) a first burst value and (ii) a first gap value;

a control circuit configured to generate an idle signal (i) in a transmit state for a first duration determined by said first burst value and (ii) in an idle state for a second duration determined by said first gap value in response to a first command signal; and

a transmitter circuit configured to (i) enable transmitting while said idle signal is in said transmit state and (ii) disable transmitting while said idle signal is in said idle state.

2. (ORIGINAL) The apparatus according to claim 1, wherein (A) said writeable registers are further configured to store a second gap value and (B) said control circuit is further configured to generate said idle signal (i) in said transmit state for said first duration and (ii) in said idle state for a third duration determined by said second gap value in response to a second command signal.

3. (ORIGINAL) The apparatus according to claim 2, further comprising:

a second plurality of writeable registers configured to store (i) a second burst value and (ii) a third gap value;

a receiver circuit configured to generate a status signal having a loss state and a presence state in response to a received signal; and

a second control circuit configured to generate a first detection signal in response to detecting a predetermined number of valid bursts each separated by a valid gap in said status signal, wherein (i) each said valid burst has a fourth duration in said presence state proportional to said second burst value and (ii) each said valid gap has a fifth duration in said loss state proportional to said third gap value.

4. (ORIGINAL) The apparatus according to claim 3, wherein (A) said second writeable registers are further configured to store a fourth gap value and (B) said second control circuit is further configured to generate a second detection signal in response to detecting said predetermined number of said valid bursts each separated by a second valid gap in said status signal, wherein said second valid gap has a sixth duration in said loss state proportional to said fourth gap value.

5. (CURRENTLY AMENDED) The apparatus according to claim ~~1~~ 3, wherein said control circuit comprises:

a burst counter configured to count a first number of clock cycles while said idle signal is in said transmit state; and

a first compare circuit configured to compare said first number of clock cycles to said first burst value, wherein said control circuit is further configured to set said idle signal to said idle state in response to said first number of clock cycles equaling said first burst value.

6. (ORIGINAL) The apparatus according to claim 5, wherein said control circuit further comprises:

a gap counter configure to count a second number of clock cycles while said idle signal is in said idle state; and

a second compare circuit configured to compare said second number of clock cycles to said first gap value, wherein said control circuit is further configured to set said idle signal in said transmit state in response to said second number of clock cycles equaling said second burst value.

7. (ORIGINAL) The apparatus according to claim 6, wherein said control circuit further comprises a third compare circuit configured to compare said second number of clock cycles to a second gap value, wherein said control circuit is further

configured to set said idle signal to said transmit state in response to said second number of clock cycles equaling said second gap value.

8. (ORIGINAL) The apparatus according to claim 1, wherein said first duration is variable in a first range from 144 to 176 bit transmit periods in response to said first burst value.

9. (ORIGINAL) The apparatus according to claim 8, wherein said second duration is variable in a second range from 432 to 528 bit transmit periods in response to said first gap value.

10. (CURRENTLY AMENDED) An apparatus comprising:

a plurality of writeable registers configured to store (i) a first burst value and (ii) a first gap value;

a receiver circuit configured to generate a status signal having a loss state and a presence state in response to a received signal; and

a control circuit configured to generate a first detection signal in response to detecting a predetermined number of valid bursts each separated by a valid gap in said status signal, wherein (i) each said valid burst has a <u>first</u> duration in said presence state proportional to said first burst value and (ii) said

each valid gap has a second duration in said loss state proportional to said first gap value.

11. (ORIGINAL) The apparatus according to claim 10, wherein (A) said writeable registers are further configured to store a second gap value and (B) said control circuit is further configured to generate a second detection signal in response to detecting said predetermined number of said valid bursts each separated by a second valid gap in said status signal, wherein said second valid gap has a third duration in said loss state proportional to said second gap value.

12. (ORIGINAL) The apparatus according to claim 11, further comprising:

a second plurality of writeable registers configured to store (i) a second burst value, (ii) a third gap value and (iii) a fourth gap value;

a second control circuit configured to generate an idle signal (A)(i) in a transmit state for a fourth duration determined by said second burst value and (ii) in an idle state for a fifth duration determined by said third gap value in response to a first command signal and (B)(i) in said transmit state for said fourth duration and (ii) in said idle state for a sixth duration

determined by said fourth gap value in response to a second command signal; and

a transmitter circuit configured to (i) enable transmitting while said idle signal is in said transmit state and (ii) disable transmitting while said idle signal is in said idle state.

13. (ORIGINAL) The apparatus according to claim 10, wherein said control circuit comprises:

a burst counter configured to count a first number of clock cycles while said status signal is in said present state; and

a first compare circuit configured to indicate one of said valid bursts when said first number of clock cycles equals said first burst value.

14. (ORIGINAL) The apparatus according to claim 13, wherein said control circuit further comprises:

a gap counter configured to count a second number of clock cycles while said status signal is in said loss state; and

a second compare circuit configured to indicate one of said valid gaps when said second number of clock cycles equals said first gap value.

15. (CURRENTLY AMENDED) The apparatus according to claim 14, wherein said control circuit further comprises a third compare circuit configured to indicate a second valid gap when said second number of clock cycles equals a ~~second~~ gap number.

16. (ORIGINAL) The apparatus according to claim 15, wherein said control circuit further comprises a sequence circuit configure to (i) generate said first detection signal in response to detecting said predetermined number of said valid bursts each separated by said valid gap in said status signal and (ii) generate a second detection signal in response to detecting said predetermined number of said valid bursts each separated by said second valid gap in said status signal.

17. (ORIGINAL) The apparatus according to claim 16, further comprising a detection circuit configured to detect a transition of said status signal between said present state and said loss state to identify a first completion of said first duration and a second completion of said second duration.

18. (ORIGINAL) The apparatus according to claim 10, wherein said first duration is variable in a first range from 144 to 176 bit reception periods in response to said first burst value.

19. (CURRENTLY AMENDED) The apparatus according to claim 18, wherein said second duration is variable in a second range from 432 to 528 bit reception periods in response to said first gap value.

20. (ORIGINAL) An apparatus comprising:

means for writeably storing (i) a first burst value and (ii) a first gap value;

means for generating an idle signal (i) in a transmit state for a first duration determined by said first burst value and (ii) in an idle state for a second duration determined by said first gap value in response to a first command signal; and

means for (i) enabling transmitting while said idle signal is in said transmit state and (ii) disabling transmitting while said idle signal is in said idle state.